

Course Project for Digital Design.

Academic Year 2021-2022

Guide : Prof. Abhay Chopde.

Name of Students : Shreyash Bhatkar, Ansh Magon, Varad Ashtekar and Pranjali Balikai.

**Design and Implementation of Universal Barre Shifter with proposed Synthesis.**

**Abstract: Data shifting and rotation is very important aspect in any modern day microprocessor. It can be persuaded as the backbone of the computationality of the micro-processing units. For that purpose we implement a barrel shifter.A barrel shifter is a logic circuit that changes the amount by which a word is shifted. It contains a control input that defines how many bit places it shifts. A barrel shifter is made up of a series of shift multiplexers, each of which shifts a word by 2k bit positions for varying values of k. A barrel shifter may complete the shift in a single clock cycle, which gives it a significant advantage over a basic shifter, which can shift n bits in n clock cycles. It is used in combination with the arithmetic logic unit (ALU) of a processor or is included in the ALU itself. In this paper we propose the design of a 4 Bit barrel shifter using Verilog HDL. The paper also aims to propose synthesis which the authors inferred from various resources. That will lead for improvement in the design of the 4 Bit barrel shifter proposed into this paper.**

**Keywords: Universal Barrel Shifter, Hardware Description Language, Verilog, Bit-Shifting, Bit Rotation, ALU and SIMD.**

*INTRODUCTION*

A barrel shifter is a type of digital logic that may shift a data word by a defined number of bits without using any sequential logic, simply pure concurrent logic. One of the key components of an automated logical unit or many fundamental electronics circuit design is indeed the barrel shifter.

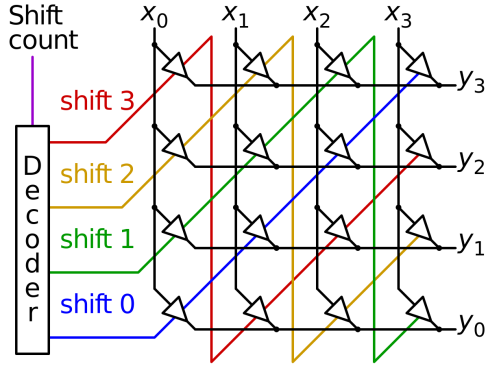


Fig.1.1 Shift visualization of Barrel shifter

The primary function of a barrel shifter is to shift bits in a single clock. In a barrel shifter, only combination logic or circuits are used, but in a regular shift register, which would only move bit stream left or right by one bit per clock input, sequential circuits are used to shift the data bit by bit rather than in a single Clock pulse, as in a barrel shifter.This is indeed a key distinction between a standard shifter and a barrel shifter. 4-bit A universal barrel shifter is a circuit that can shift one or four bits left or right arithmetic or logically in a single command. This is the benefit of employing a universal barrel shifter, since no clock pulses or sequential logic are necessary, and the combinatorial circuits accomplish the entire job.

Since media applications have grown in importance, SIMD (SingleInstruction-Multiple-Data) ISA (Instruction Set Architecture) enhancements that use sub-word parallelism have been introduced in several generic microprocessors [1]. SIMD ISAs boost DSP and multimedia efficiency of any proposed algorithm by 1.6–11.66 times over nonSIMD codes by performing similar operations on several data sets of varying sizes in parallel [2]. As a result, numerous execution units of varying sizes should be put in place to support them. Because they prioritise performance over hardware cost, high-performance general-purpose microprocessors implement SIMD ISAs by replicating functionalities [3]. Some functional unit designs are suggested to handle packed data with modest hardware overheads in adders and multipliers for more costeffective implementations [4],[5].

The following computationality is implemented by the authors in this project.

Table [1] LOGICAL LEFT SHIFT

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0 | 0 | D3 | D2 | D1 | D0 |
| 0 | 1 | D2 | D1 | D0 | 0 |
| 1 | 0 | D1 | D0 | 0 | 0 |
| 1 | 1 | D0 | 0 | 0 | 0 |
| S1 | S0 | P3 | P2 | P1 | P0 |

We can assume that d0, d1, d2, and d3 are input bits, with d0 serving as the LSB bit.

S1 and S0 are the select pins, while P3, P2, P1, and P0 are the intended outputs, with P3 being the MSB

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| S1 | S0 | P3 | P2 | P1 | P0 |
| 0 | 0 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | D3 | D2 | D1 |
| 1 | 0 | 0 | 0 | D3 | D2 |
| 1 | 1 | 0 | 0 | 0 | D3 |

Table [2] Logical Shift Right:

Table [3] Rotate Left:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| S1 | S0 | P3 | P2 | P1 | P0 |
| 0 | 0 | D3 | D2 | D1 | D0 |
| 0 | 1 | D2 | D1 | D0 | D3 |
| 1 | 0 | D1 | D0 | D3 | D2 |
| 1 | 1 | D0 | D3 | D2 | D1 |

Table [4] Rotate Right:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| S1 | S0 | P3 | P2 | P1 | P0 |
| 0 | 0 | D3 | D2 | D1 | D0 |
| 0 | 1 | D0 | D3 | D2 | D1 |
| 1 | 0 | D1 | D0 | D3 | D2 |
| 1 | 1 | D2 | D1 | D0 | D3 |

Because each of the blocks has four output bits, a total of 16 combinations of outputs are predicted because they may be modified like four modes of the circuit.

Graphical user interface, calendar

Description automatically generated

This Logical result is sent to the Barrel Shifter circuit, which is built using a 4:1 Multiplexer. Y0 and Y15 are the LSB and MSB bits, respectively. The circuit's modes are S1 and S0. We can use the truth table above to evaluate the expressions for each output and then use that expression to build a combinational logic circuit.

***Literature Review:***

The architecture of MUX-based 4-bit barrel shifters on 16nm FINFET technology is proposed in this paper. The proposed 4-bit MUX architecture consumes less power due to less switching activity. This circuit enables bidirectional rotation of a four-bit word by 0, 1, 2, and 3 bits. The power consumption of the barrel shifter designed with FINFET is reduced by 25%, the delay is reduced by 36%, and the power delay product is reduced by 9%. (PDP).

When compared to conventional MOSFET architectures, the power consumed, delay and Power Delay Product (PDP), RMS value, and peak to peak power are all reduced. Using 16nm FINFET Technology, the proposed architecture is designed and simulated in HSPICE. Because of its low power consumption and delay, 2 MUX is used in the design of the MUX Tree architecture.

It has been observed [1] that when a complementary metal oxide semiconductor is downscaled beyond a size of 22 nano metres, there is an increase in its power requirement. This increase in power requirement has caused over heating in components. Replacing complementary metal oxide semiconductor with FinFET’s for universal barrel shifter has shown increase in performance. For CMOS application it was observed that there was a short channel effect. This short channel effect was studied [2] and results show that FinFET proves to perform better.

The FinFET technology has delivered superior scalability thus allowing more suppression the leakage current observed. This enhancement was seen because of higher intrinsic gain and lower channel length modulation. Analysis [3] of FinFET’s on the leakage current have shown extraordinary results. This approach shall synthesize a faster barrel shifter, which in turn can reduce the delay of design without any increase in area. Using Gaussisan dopping [4] inside Trigate junction less FinFETS’s delivers high performance. This approach has delivered better electrical characteristics of potential distribution. The continuous downscaling of MOSFET’s [4] has shown an increase or decrease in performance and increased density in the circuit which s started by the Moore’s law. To tackle the decrease in performance, modifications have been made in the circuits. Th use of double fate, surrounding gate and trigate MOSFET’s have been used. All this was done to reduce the short channel effect [2] .

When dealing with a loss less information environment [5], that is a reversible logic in the synthesis of logic. Due to the presence of lower power dissipation, there is a need to design the components with reversible gates. This reversible gate has the unique characteristic of one-to-one mapping for both output and input vectors. Logic reversibility can regain the bit loss [5]. The limitation is that it is unable to find any error or noise.

[21]The proposed paper demonstrates four barrel shifter designs: mux-based data-reversal, mask-based data-reversal, mask-based two's complement, and masked-based one's complement. Area and delay estimates, taken from synthesis of the structural level VHDL, indicate that data-reversal barrel shifters outperform the other designs. As the operand size increases, the delay of the shifters increases as O(log(n)) and their area increases as O(n log(n))

In comparison with a purely MUX based barrel shifter, a combinational logic circuit can create the barrel shifter using multiplexers, decoders and logic gates. MUX-based architecture is used to design the Barrel Shifter, which requires less switching activity. This system uses 16nm FinFET technology. [22]The paper shows that power consumed, delay, Power Delay Product (PDP), RMS value, peak to peak power, and power delay are reduced when compared with conventional MOSFET architectures. Thus finFET MUX based Barrel shifters appear more eminent than conventional MOSFET designs.

[4] The proposed 4-bit MUX architecture consumes less power due to less switching activity. This circuit enables bidirectional rotation of a four-bit word by 0, 1, 2, and 3 bits. The power consumption of the barrel shifter designed with FINFET is reduced by 25%, the delay is reduced by 36%, and the power delay product is reduced by 9%. (PDP).

When compared to conventional MOSFET architectures, the power consumed, delay and Power Delay Product (PDP), RMS value, and peak to peak power are all reduced. Using 16nm FINFET Technology, the proposed architecture is designed and simulated in HSPICE. Because of its low power consumption and delay, 21 MUX is used in the design of the MUX Tree architecture.

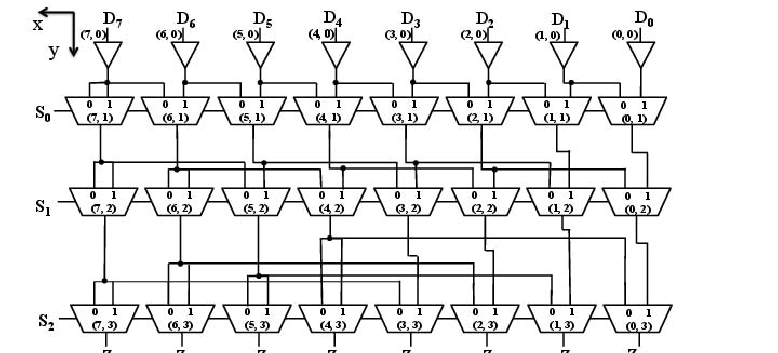
[18]Implementation of multiplicationthrough barrel shifters can save around 85% of time and occupy fewer bits than repetitive addition. Multiplication follows the principle of binary addition. Any one of the operands in multiplication is represented in terms of summation of two’s exponents and followed by a set of left shift operations. Similarly in division, the set of right shift instructions are needed. Both division and multiplication operations can be implemented together using bidirectional barrel shifter with appropriate reversal logic.

The main aim of upcoming designs is increase in performance without requiring more power consumption. In[20] the reversible bidirectional barrel shifter capable of performing rotation and shifting operations is designed and simulated through Verilog HDL.This design was made using Fredkin and Feyman gates.

The area-efficient circuits with high performance is possible with adaptation of layout generation environments[20]. In this work several different 32-bit barrel shifter layout implementations are evaluated, in thecontext of developing area- and performance-efficient methodslayout methods. The wired is used as frontend and Cadence SoC Encounter is used as backend to generate efficient layouts.

*Architecture*

The given figure below presents the block diagram of a universal barrel shifter. It is an architecture an 8-bit barrel shifter with left and right vectors. In addition, it also consists of 8-to-8 cross bar network. A multiplexer is used to select each byte between source 1 operand and the second source operand. Using mask logic, the result is obtained. Each 8-bit barrel shifter is supposed to shift a byte of source 1 operand. The shift counts values placed on the operand of second source. Shifting rightward, bits from left vector are placed towards the leftmost position. Leftward shifting, the vectors on the right are placed on rightmost position. The left vector was selected from a left byte source of the first operand. All zero bits that depend on the size of the data.



Block diagram 1.2: Universal barrel shifter

The outputs of the barrel shifter were transferred to an 8-to-8 crossbar network bundled with one byte unit. The cross network was implemented with M-input multiplexers. Shifting by single bytes was executed through the crossbar network. Reorganizing instruction are executed by utilizingsigned/ unsigned, repeat, replace, convert endian and many more. Multiplexers are used to select the bits between the two sources for both signed and unsigned pack, replace instruction and others. The circuits for masking logic were required in masking the shifted bytes and the saturating packed values. It could select either one of the following: signed maximum value, signed minimum values , all the ones, all the zeros and the output of all multiplexers. Signed maximum and minimum values were selected. All zeroes and all the ones are selected when a value is extended with the sign or zero by hit operations.

CIRCUIT DIAGRAM

**4:1 Multiplexer**

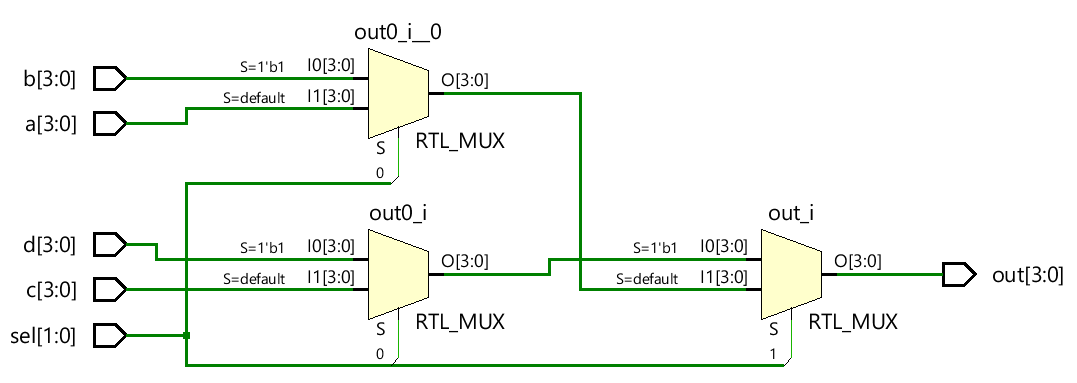


Figure 2.1: 4:1 MUX

the Multiplexer will either select a,b,c or d based on the logic or flag at the select line.

Diagram, schematic

Description automatically generated

Figure 2: Universal Barrel Shifter with Inputs pins

Universal Barrel Shifter with Inputs pins as S1, S0, D0, D1, D2, D3 and gnd. With output as P3, P2, P1 and P0. P0 being the LSB

Chart

Description automatically generated with medium confidence

Diagram, schematic

Description automatically generatedFigure 3: Left Logic of Circuit

The Left logic Which is used in the main circuit where the inputs are being taken and after processing given to the 4:1 Multiplexer

Results:

For the Mode 2nd Which is Shift Right Logical.

A picture containing background pattern

Description automatically generated

For the Mode 1st Shift Left Logical

Table

Description automatically generated with medium confidence

# Observations:

It can be observed that the waveform of the results are changing as per expectation of the logic as the mode and select pins changes. No Time Delay is present in between the transition of input change to the output change, the process is instantaneous. This is the advantage of Universal Barrel Shifter over the Universal Shift Registers. No clock pulses are required for the design of the circuit. Only Combinational logics are used.

Proposed Synthesis:

Comparing the planned architecture's occupied area and time delay to those of a typical barrel.

shifters, as well as the parallel shifter presented in [12]. The parallel shifter just performs shift instructions and is not required. extra pack unit that performs data reorganisation operations Because the parallel shifter can only shift a packed. In order to implement, data with similar shift amounts must be used. The same features as the universal shifter a 64-bita barrel shifter, a 32-bit shifter, two 16-bit shifters, and four four-bit shifters. It is necessary to use 8-bit shifters and a pack unit [3].

Conclusion:

From the obtained Simulation results on Xilinx ISE through FPGA Spartan 3, the outputs can verify with the expected logic in the Truth table.A Universal Barrel Shifter can be designed with help of basic logic units and 4:1 Multiplexers.Bits can be shifted in one go from 1 to 4 bits in either of the directions and with either of the type Logical or rotate. Without using Sequential circuits, Universal shifter architecture was proposed that can execute various vector shifts with individual shift counts as well as various data reorganization operations of the current SIMD ISA extensions. Combinational logic circuits such as multiplexers, decoders, and logic gates are useful when designing a barrel shifter, whereas a purely MUX based barrel shifter has a lower power and delay. Digital circuits that use shift registers can be replaced with these high speed barrel shifters in Arithmetic and Logic Units (ALU) and Digital Signal Processors, for example, so that the area, power and delay can be reduced, resulting in better performance. The universal shifter reduces the amount of occupied space by 56% and delays the program by 6% compared to conventional implementations with the same functionality. Based on the simulation results obtained using Xilinx ISE and FPGA Spartan 3, the outputs may verify the logic in the Truth table. A Universal Barrel Shifter can be designed with the help of basic logic units and 4:1 multiplexers. Bits can be shifted in one go from 1 to 4 in either direction without using a sequential circuit. This shifter architecture adds various features with only 27% of the total area and 1.43 ns delay over a 64-bit barrel shifter. Using the proposed universal shifter architecture, SIMD ISA extensions to microprocessors can be implemented at a reasonable cost.

**References**

1. Lee, R. B.: Multimedia extensions for general-purpose processors. Proc. IEEE Workshop on Signal Processing Systems (1997), 9–23.
2. Nguyen, H.; John, L. K.: Exploiting SIMD parallelism in DSP and multimetia algorithms using the AltiVec technology. Proc. ACM Int. Sym. on Supercomputing (1999), 11–20.
3. Schmookler, M. S.; Putrino, M.; Roth, C.; Sharama, M.; Mather, A.; Tyler, J.; Nguyen, H. V.; Pham, M. N.; Lent, J.: A low-power, high-speed implementation of a PowerPC microprocessor vector extension. 14th IEEE Symp. On Computer Arithmetic (1999), 12–21.
4. E. Lehman, Y. Watanabe, J. Grodstein and H. Harkness, "Logic decomposition during technology mapping", International Conference on Compuer-Aided Design, pp. 264-271, 1995.
5. C. L. Liu, Introduction To Combinatorial Mathematics, McGraw-Hill, Inc., 1968.
6. R. Murgai, R. K. Brayton and A. L. Sangiovanni-Vincentelli, "An improved synthesis algorithm for multiplexer-based pgas", Design Automation Conference, pp. 380-386, 1992.
7. S. Thakur, D. F. Wong and S. Krishnamoorthy, "Delay minimal decomposition of multiplexers in technology mapping", Design Automation Conference, 1996.
8. C.-Y. Tsui, M. Pedram and A. M. Despain, "Technology decomposition and mapping targeting low power dissipation", Desgin Automation Conference, pp. 68-73, 1993.
9. Michael J. Schulte and E. George Walters III, Computer Architecture and Arithmetic Laboratory ,Computer Science and Engineering Department, Lehigh University Bethlehem, PA 18015, USA
10. Abhijit Asati and Chandrashekhar, “VLSI Implementation of a High Performance Barrel Shifter Architecture using Three Different Logic Design Styles” , International Journal of Recent Trends in Engineering, Vol. 2, No. 7, pp22-26, November 2009 .
11. Priyanka Agrawal and Dr. Rajesh Mehra, “Design and Performance Analysis of Barrel Shifter Using 45nm Technology”, IOSR Journal of VLSI and Signal Processing (IOSR-JVSP), Volume 6, Issue 3, Ver. I, PP 38-44, May. -Jun. 2016.

[12]Lin, D. C.; Minocha, P.; Peleg, A. D.; Yaari, Y.; Mittal, M.; Mennemeier, L. M.; Eitan, B.: Apparatus for performing packed shift operations. US patent 6,275,834 (2001).

[13] R. Rajalakshmi and P. Aruna Priya, "Design and analysis of a 4-bit low power universal Barrel-shifter in 16nm FinFET technology," 2014 IEEE International Conference on Advanced Communications, Control and Computing Technologies, 2014, pp. 527-532, doi: 10.1109/ICACCCT.2014.7019141.

[14] A. N. Bhoj and N. K. Jha, "Design of Logic Gates and Flip-Flops in High-Performance FinFET Technology," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 21, no. 11, pp. 1975-1988, Nov. 2013, doi: 10.1109/TVLSI.2012.2227850.

[15] S. Das and S. P. Khatri, "Timing-driven decomposition of a fast barrel shifter," 2007 50th Midwest Symposium on Circuits and Systems, 2007, pp. 574-577, doi: 10.1109/MWSCAS.2007.4488648

[16] Mitra, Sajib & Chowdhury, Ahsan Raja. (2015). Optimized Logarithmic Barrel Shifter in Reversible Logic Synthesis. Proceedings of the IEEE International Conference on VLSI Design. 2015. 441-446. 10.1109/VLSID.2015.80.

[17] Web resource URL:

<https://www.iosrjournals.org/iosr-jvlsi/papers/vol6-issue3/Version-1/G0603013844.pdf>

Last accessed on: 05/01/2022

[18] M. P.R. and S. Asokan, "Adapting Barrel Shifter at Compilation Level for Efficient Implementation of Multiplications," 2012 International Conference on Advances in Computing and Communications, 2012, pp. 162-165, doi: 10.1109/ICACC.2012.37.

[19]A. Bardizbanyan, K. P. Subramaniyan and P. Larsson-Edefors, "Generation and Exploration of Layouts for Area-Efficient Barrel Shifters," 2010 IEEE Computer Society Annual Symposium on VLSI, 2010, pp. 454-455, doi: 10.1109/ISVLSI.2010.73.

[20] O. Anjaneyulu, T. Pradeep and C. V. K. Reddy, "Design and implementation of reversible logic based bidirectional barrel shifter," 2012 10th IEEE International Conference on Semiconductor Electronics (ICSE), 2012, pp. 490-494, doi: 10.1109/SMElec.2012.6417193.

[21]R. Pereira, J. A. Mitchell, and J. M. Solana, \Fully Pipelined TSPC Barrel Shifter for High-speed Applications," IEEE Journal of Solid State Circuits, vol. 30, pp. 686{690, June 1995

[22] Abhijit Asati I and Chandrashekhar "A purely mux based high speed barrel shifter VLSI implementation using three different logic design style" Mechanical Engineering and Technology, AISC 125,pp. 639-646.